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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/629,095	07/29/2003	Wolfgang Ramin	TID-32348 6377		
23494 759	90 04/05/2005		EXAMINER		
	RUMENTS INCORPOR	GEBREMARIAM, SAMUEL A			
P O BOX 65547 DALLAS, TX		ART UNIT	PAPER NUMBER		
			2811		
			DATE MAILED: 04/05/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary		Application	Application No. Applicant(s)				
		10/629,09	95	RAMIN, WOLFGANG			
		Examiner		Art Unit			
<u></u>			Gebremariam	2811			
۔ Period fo	 The MAILING DATE of this communical Reply 	tion appears on the	cover sheet with the	correspondence ad	ddress		
THE N - Exten after S - If the - If NO - Failure Any re	DRTENED STATUTORY PERIOD FOR MAILING DATE OF THIS COMMUNICATION of time may be available under the provisions of 3 (slX (6) MONTHS from the mailing date of this communication period for reply specified above is less than thirty (30) deperiod for reply is specified above, the maximum statute is to reply within the set or extended period for reply will, exply received by the Office later than three months after department adjustment. See 37 CFR 1.704(b).	ATION. TOFR 1.136(a). In no every cation. ays, a reply within the state ory period will apply and wi by statute, cause the app	ent, however, may a reply be to story minimum of thirty (30) da Il expire SIX (6) MONTHS fror lication to become ABANDON	imely filed ays will be considered time in the mailing date of this of ED (35 U.S.C. § 133).			
Status							
1)⊠	Responsive to communication(s) filed o	on <u>29 December 2</u>	<u>004</u> .				
•	•	☐ This action is n					
•	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Dispositi	on of Claims			•			
5)□ 6)⊠ 7)□	Claim(s) <u>1-15</u> is/are pending in the app (4a) Of the above claim(s) is/are Claim(s) is/are allowed. Claim(s) <u>1-15</u> is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction	withdrawn from co					
Application	on Papers						
9) 🗆 -	The specification is objected to by the E	Examiner.					
•	☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
	Replacement drawing sheet(s) including th The oath or declaration is objected to b						
Priority u	nder 35 U.S.C. § 119						
a)[Acknowledgment is made of a claim for All b) Some * c) None of: 1. Certified copies of the priority do 2. Certified copies of the priority do 3. Copies of the certified copies of application from the International see the attached detailed Office action for	ocuments have been been been been the priority documents Bureau (PCT Rul	en received. en received in Applica ents have been receive e 17.2(a)).	ition No ved in this Nationa	l Stage		
Attachmen							
	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTC) ₋ 048\	4) Interview Summa Paper No(s)/Mail				
3) Inform	e of Draitsperson's Patent Drawing Review (PTC nation Disclosure Statement(s) (PTC-1449 or PT r No(s)/Mail Date		5) Notice of Informal 6) Other:		O-152)		

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamzehdoost et al., US patent No. 5,371,321.

Regarding claim 1, Hamzehdoost teaches (fig. 2) an encapsulated chip assembly comprising (refer to fig. 2): a baseplate (52), a chip (56) attached to the baseplate in such a way that its contact surfaces (the top surface of 56) face away from the baseplate (52), a layer (76) of a conductive material applied to the baseplate (52) and arranged around the chip (56) and having a support surface facing away from the baseplate (52) (the top layer of 76 supports the structures above it, therefore layer 76 has a support surface facing away from the base plate), which is at least as high as the surface of chip (56), a cover plate (68) arranged on the layer of conductive material (76), whose one side, opposing the chip (56), being provided with one or more conductive surfaces (70,72), which are arranged in such a way that they form an electrical connection between the chip (56, col. 5, lines 7-25) and the layer of conductive material (76), the support surface of the layer (76) serving as a support for the cover plate (68).

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Regarding claim 6, Hamzehdoost teaches the entire claimed structure of claim 1, above including both the baseplate (52, col. 4, lines43-50) and the cover plate (68, col. 4, lines 63-67) each consist of a flexible material.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost in view of Nakaoka et al. US patent No. 6,583,512.

Regarding claim 2, Hamzehdoost teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the chip is surrounded by a filler material that fills the open space between the baseplate and the cover plate.

Nakaoka teaches the use of a filler material (30, col. 11, lines 64-67) in order to fill the space between the semiconductor devices (fig. 8c).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the filler material taught by Nakaoka in the structure of Hamzehdoost in order to further seal the device.

Regarding claim 3, Hamzehdoost teaches substantially the entire claimed structure of claims 1 and 2 above including further comprising an electrically conductive glue (74), which is to establish both the electrical and the mechanical connections between the contact surfaces of the chip (56) and of the cover plate (68).

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Regarding claim 4, Hamzehdoost teaches substantially the entire claimed structure of claims 1 and 2 above including further comprising an anisotropically conductive film (30, col. 11, lines 64-67, Nakaoka) (ACF), which serves to establish both an electrical and a mechanical connection between the contact surfaces of the chip and the conductive surface.

Regarding claim 5, Hamzehdoost teaches substantially the entire claimed structure of claims 1 and 2 above including the filler material consists of the anisotropically conductive film (col. 11, lines 64-67, Nakaoka).

5. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost.

Regarding claims 7-8, Hamzehdoost teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the height of the chip is so low that it is rendered flexible or has a thickness of less than 50 micrometer. Since most integrated circuits use silicon Hamzehdoost teaches a chip that consists mainly of silicon.

Furthermore parameters such as height in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the height of the IC of Hamzehdoost as claimed in order to form a device that is easily packaged.

6. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost, in view of Loeffler et al. US patent No. 5,838,074.

Regarding claim 9, Hamzehdoost teaches substantially the entire claimed structure of claims 1 and 2 above except explicitly stating that the chip comprises a transponder.

Loeffler teaches that a transponder can be integrated as an IC device (transponder IC, col. 3, lines 16-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the transponder device taught by Loeffler in the structure of Hamzehdoost in order to package a transponder device that is integrated with an integrated circuit.

Regarding claim 10, Hamzehdoost teaches substantially the entire claimed structure of claims 1 and 2 above including the conductive layer comprises an aerial.

The combined structure Hamzehdoost and Loeffler teaches a transponder that is integrated as an IC device. Since a transponder in general is equipped with an antenna structure, the combined structure of Hamzehdoost and Loeffler would inherently have an aerial that is made of a conductive material.

Regarding claim 11, Hamzehdoost teaches substantially the entire claimed structure of claims 1, and 9-10 above except explicitly stating that a chip having a transponder attached to the baseplate.

Since the combined structure of Hamzehdoost and Loeffler teaches that a transponder can be integrated as an IC device, it would have been obvious to one of Art Unit: 2811

ordinary skill in the art at the time the invention was made to incorporate the transponder device taught by Loeffler in the structure of Hamzehdoost in order to package a transponder device that is integrated with an integrated circuit.

7. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamzehdoost, Nakaoka and in view of Loeffler.

Hamzehdoost teaches substantially the entire claimed structure of claims 1, 3, 7-8 and 9-10 above including the height of the chip is so low that it is rendered flexible.

Response to Arguments

8. Applicant's arguments filed 12/29/04 have been fully considered but moot in view the new grounds of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG March 22, 2005

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SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800